

What is claimed is:

1. A microcontroller operating in synchronization with a clock, comprising:

5 an arithmetic unit operating in synchronization with the clock;

an internal resource being connected to the arithmetic unit via a bus, and having at least a bus interface and an internal circuit which operates in synchronization with 10 the clock; and

a system resource prescaler which generates, from the clock, an operation permission signal denoting an operation permission state in m cycles out of n cycles of the clock ($m = < n$), and supplies the operation permission signal to 15 the internal circuit of the internal resource,

wherein the internal circuit operates in synchronization with the clock when the operation permission signal denotes the operation permission state.

20 2. The microcontroller according to claim 1,

wherein the bus interface of the internal resource operates in synchronization with the clock.

3. The microcontroller according to claim 1,

25 wherein the internal resource includes a communication macro controlling communication with outside, and an internal circuit of the communication macro includes a

counter which generates a communication control clock.

4. The microcontroller according to claim 1,
wherein the internal resource comprises a pulse
5 generation macro generating a control pulse, and an
internal circuit of the pulse generation macro comprises
a counter controlling a generation timing of the control
pulse.

10 5. The microcontroller according to claim 1,
wherein the system resource prescaler comprises a
register storing the values m and n, and the register can
be set alterably.

15 6. The microcontroller according to claim 5,
wherein the system resource prescaler comprises a
settable operation control register indicative of either
a first operation state in which the operation permission
signal is set constantly to the operation permission state
20 or a second operation state in which the operation
permission signal is set to the operation permission state
in the m cycles out of the n cycles.

7. The microcontroller according to claim 1,
25 wherein the system resource prescaler dispersively
allocates the m cycles throughout the n cycles.

8. The microcontroller according to claim 1,
wherein the system resource prescaler comprises a
preceding-stage prescaler and a succeeding-stage
prescaler which generates a succeeding-stage operation
5 permission signal using a preceding-stage operation
permission signal which is generated and supplied from the
preceding-stage prescaler, and the succeeding-stage
operation permission signal is supplied to the internal
circuit of the internal resource.

10

9. The microcontroller according to claim 8,
wherein the preceding-stage prescaler and the
succeeding-stage prescaler respectively comprise
registers storing the values m and n, and the registers
15 can be set alterably.

10. The microcontroller according to claim 9,
wherein the succeeding-stage prescaler further
comprises an operation control register in which can be
20 set any one of a first operation state enabling the
succeeding-stage operation permission signal to be set
constantly to an operation permission state, a second
operation state enabling the succeeding-stage operation
permission signal to be set to the operation permission
25 state in the m cycles out of the n cycles, and a third state
generating the succeeding-stage operation permission
signal irrespective of the states of the preceding-stage

operation permission signal.

11. A microcontroller operating in synchronization with a clock, comprising:

5 an arithmetic unit operating in synchronization with the clock;

 an internal resource being connected to the arithmetic unit via a bus, and having at least a bus interface and an internal circuit operating in synchronization with the 10 clock; and

 a system resource prescaler which generates, from the clock, an operation permission signal having a lower frequency than the clock, and supplies the operation permission signal to the internal circuit of the internal 15 resource,

 wherein the internal circuit operates in synchronization with the clock when the operation permission signal denotes the operation permission state.

20 12. The microcontroller according to claim 11,

 wherein the operation permission signal is controlled to be set to the operation permission state on a cycle-by-cycle basis of the clock.

25 13. The microcontroller according to claim 12,

 wherein the operation permission signal is set to the operation permission state in m cycles out of n cycles of

the clock, and the values n and m can be set alterably.